REMARKS

The Examiner's Action mailed on July 8, 2005 has been received and its contents carefully considered.

In this submission, Applicant has amended independent claims 9 and 13. Claims 10 and 14 are cancelled. Claims 16-19 are added for further protection. After entry of the foregoing amendments, claims 9, 11, 13 and 16-19 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 9 to 11 were tentatively rejected under 35 U.S.C. 103(a) as allegedly obvious over *Ota et al.* (JP 06-084946), and *Licari et al.* (U.S. Patent No. 5,485,038). Claim 10 has been cancelled. For at least the reasons set forth below, Applicant submits that the rejection of claims 9 and 11 should be withdrawn.

Applicant's independent claim 9 recites a thin film transistor (TFT) structure, which includes a plurality of stacked structures, a photo-imagable layer, a source electrode and a drain electrode, a passivation layer, and a transparent electrode. The stacked structures are disposed on a substrate and include a first conducting layer, an insulation layer, and an amorphous silicon layer. The **photo-imagable layer** is disposed between the stacked structures so as to be in **contact with the first conducting layer**, the insulation layer, the **amorphous silicon layer** and the **ohmic contact layer**. The **source electrode and drain electrode are disposed on the photo-imagable layer**. The source electrode is connected to a portion of the amorphous silicon layer and the drain electrode is connected to another portion of the amorphous silicon layer. The passivation layer is disposed on the amorphous silicon layer, the source electrode and the drain electrode. The **transparent electrode** is disposed **on the passivation layer** and electrically connected to one of the source electrode and the drain electrode.

In contrast, *Ota et al.* disclose an active matrix liquid crystal device and method for manufacturing same. An insulating film 16 on a glass board 1 has a groove and a black matrix layer 2, formed in the groove, is also disposed on the glass board 1. The black matrix layer 2, an intermediate insulating layer 17, a gate electrode 3, a gate insulating film 4, a semiconductor channel layer 5, ohmic contact layers 6S, 6D are sequentially formed. (see Abstract; and FIG. 3) Then, a transparent display electrode 7 is formed on the insulating film 16. Both of a source electrode 8 and a drain electrode 9 are formed on the gate insulating layer 4, but only the drain electrode 9 is further formed on the display electrode 7. The source electrode 8 and the drain electrode 9 covers the gate insulating film 4, the semiconductor channel layer 5, and the ohmic contact layers 6S, 6D. The passivation film 10 is formed on and covers the source electrode 8 and the drain electrode 9 (Paragraph [0018], Col. 6, lines 33-38 and 44-47; and FIGS. 12-13)

The Office Action admitted that *Ota et al.* do not show the first stacks including an ohmic contact layer and the interlayer made of photo-imagable material, but relied on the teaching of *Licari et al.* to use photo-imagable material for interlayers as taught by *Licari et al.*

However, there is no disclosure or a suggestion by *Ota et al.* that the photo-imagable layer is in contact with the first conducting layer, the insulation layer, the amorphous silicon layer and the ohmic contact layer, as recited in claim 9. *Ota et al.* disclose the amorphous silicon layer 5 formed on the gate insulating film 4 and the ohmic contact layers 6S, 6D formed thereon are covered by the source electrode 8 and the drain electrode 9. Further, the gate electrode 3 of *Ota et al.*, relied upon by the Examiner as teaching the first conducting layer, is neither contact with the photo-imagable layer nor formed on the substrate. Instead, as is clear from FIG. 3, the gate electrode 3 is formed on the intermediate insulating layer 17 and covered by the gate insulating film 4.

Moreover, *Ota et al.* fail to disclose or suggest that the source electrode and drain electrode are disposed on the photo-imagable layer, as recited in claim 9. Rather, both of the source electrode 8 an the drain electrode 9 of *Ota et al.* are formed on the gate insulating layer 4, and the drain electrode 9 is further formed on the display electrode 7 in order to supply the source electrode 8 with the charge in and out of the display electrode 7 through the semi-conductor channel layer 5. (Col. 6, lines 44-47).

In addition, the Office Action has equated the display electrode 220 disclosed by *Ota et al.* as teaching the transparent electrode of the present invention. However, as revealed in paragraph [0018], Col. 6, lines 33-38 of *Ota et al.*, the display electrode 220 in FIG. 1 is equivalent to the display electrode 7, which is formed on the insulating film 16. (FIG. 12) This contrasts with the present claims, which define that the transparent electrode is disposed on the passivation layer.

Furthermore, the secondary reference, *Licari et al.*, fails to overcome the deficiencies of *Ota et al.* Thus, neither *Ota et al.* nor *Licari et al.* disclose or suggest the claimed structure. As such, it is respectfully submitted that Applicant's independent claim 9, as well as claim 11 dependent therefrom, are patentable over the cited references.

Claims 13 and 14 have been rejected under 35 U.S.C. 103(a) as allegedly unpatentable over *Ota et al.* and *Licari et al.*, as applied to claim 9 above, and further in view of *Tsujimura et al.* (U.S. Patent Application No. 2002/0190253). Claim 14 has been cancelled. It is submitted that independent claim 13 is patentable over the cited references for at least the reasons that follow.

Applicant's independent claim 13 recites a thin film transistor (TFT) structure, which includes a plurality of first stacked structures and second stacked structures, a photo-imagable layer, a source electrode and a drain electrode, a passivation layer, and a transparent electrode.

The first stacked structures are disposed on a substrate and include a first conducting layer, an insulation layer, and an amorphous silicon layer. The second stacked structures are disposed on a substrate and include the first conducting layer. The photo-imagable layer is disposed between the first stacked structure and the second stacked structures so as to be contact with the **first conducting layer**, the insulation layer, the **amorphous silicon layer** and the **ohmic contact layer**. The **source electrode and drain electrode** are disposed **on the photo-imagable layer** and the first stacked structures. The source electrode is connected to a portion of the amorphous silicon layer and the drain electrode is connected to another portion of the amorphous silicon layer. The passivation layer is disposed on the amorphous silicon layer, the photo-imagable layer and the source electrode and the drain electrode. The transparent electrode is disposed on the passivation layer; a first portion of the transparent electrode electrically connects to one of the source electrode and the drain electrode; and a second portion of the transparent electrode electrically connects to the second conducting layer of the first stacked structures and the first conducting layer of the second stacked structure.

In contrast, there is no disclosure or a suggestion by *Ota et al.* that the photo-imagable layer is in contact with the first conducting layer, the insulation layer, the amorphous silicon layer and the ohmic contact layer, as recited in claim 13. Instead, as is clear from FIG. 3, the gate electrode 3 of *Ota et al.*, relied upon by the Examiner as teaching the first conducting layer, is formed on the intermediate insulating layer 17 and covered by the gate insulating film 4. Besides, *Ota et al.* disclose the amorphous silicon layer 5 formed on the gate insulating film 4 and the ohmic contact layers 6S, 6D formed thereon are covered by the source electrode 8 and the drain electrode 9.

Moreover, *Ota et al.* fail to disclose or suggest that the source electrode and drain electrode are disposed on the photo-imagable layer, as recited in claim 13. Rather, both of the

source electrode 8 an the drain electrode 9 of *Ota et al.* are formed on the gate insulating layer 4, and the drain electrode 9 is further formed on the display electrode 7 in order to supply the source electrode 8 with the charge in and out of the display electrode 7 through the semi-conductor channel layer 5. (Col. 6, lines 44-47).

The Office Action alleged that *Ota et al.* and *Licari et al.* show most aspects of the instant invention except the second stack structures and further points to *Tsujimura et al.* as teaching a second stack with a conductive layer to control the capacitance of the substrate.

However, neither *Licari et al* nor *Tsujimura et al.* overcome the deficiencies of *Ota et al.* As such, the claimed structure is not disclosed nor suggested by *Ota et al* alone nor in combination with *Licari et al.* and *Tsujimura et al.* It is therefore submitted that the claim 13 is patentable over the cited references. Claims 10-11 are also patentable over the cited references for at least the reasons advanced above as to the patentability of independent claim 9, from which these claims respectively depend, as well as for the additional features they recite.

For at least the foregoing reasons, the rejections of claims 9, 11, 13, and 16-19 should be withdrawn.

As a separate and independent basis for the patentability of these claims, Applicant respectfully submits that rejections fail to cite or identify a proper motivation for combining the various references relied upon. For example, in combining Licari and Ota (see paragraph 3, page 3), the Office Action actually relied upon an alleged teach of Tsujimura, stating that the combination would have been obvious "because these materials are less expensive and more efficient to use than conventional interlayer material." The, when further combining Tsujimura (see paragraph 4, page 4), the Office Action stated only that the further combination would have been obvious "to control the capacitance of the substrate." This alleged motivation is clearly improper in view of well-established Federal Circuit precedent.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicant notes that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a thin film transistor structure, as claimed by the Applicant.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art,

or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000).

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejections under 35 U.S.C. § 103, those rejections should be withdrawn.

CONCLUSION

For at least the foregoing reasons, it is submitted that this application is in condition for allowance and such a Notice, with allowed claims 9, 11, 13 and 16-19 earnestly is solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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